Approaching the One Billion Transistor Logic Product: Process and Design Challenges

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Intel Corporation

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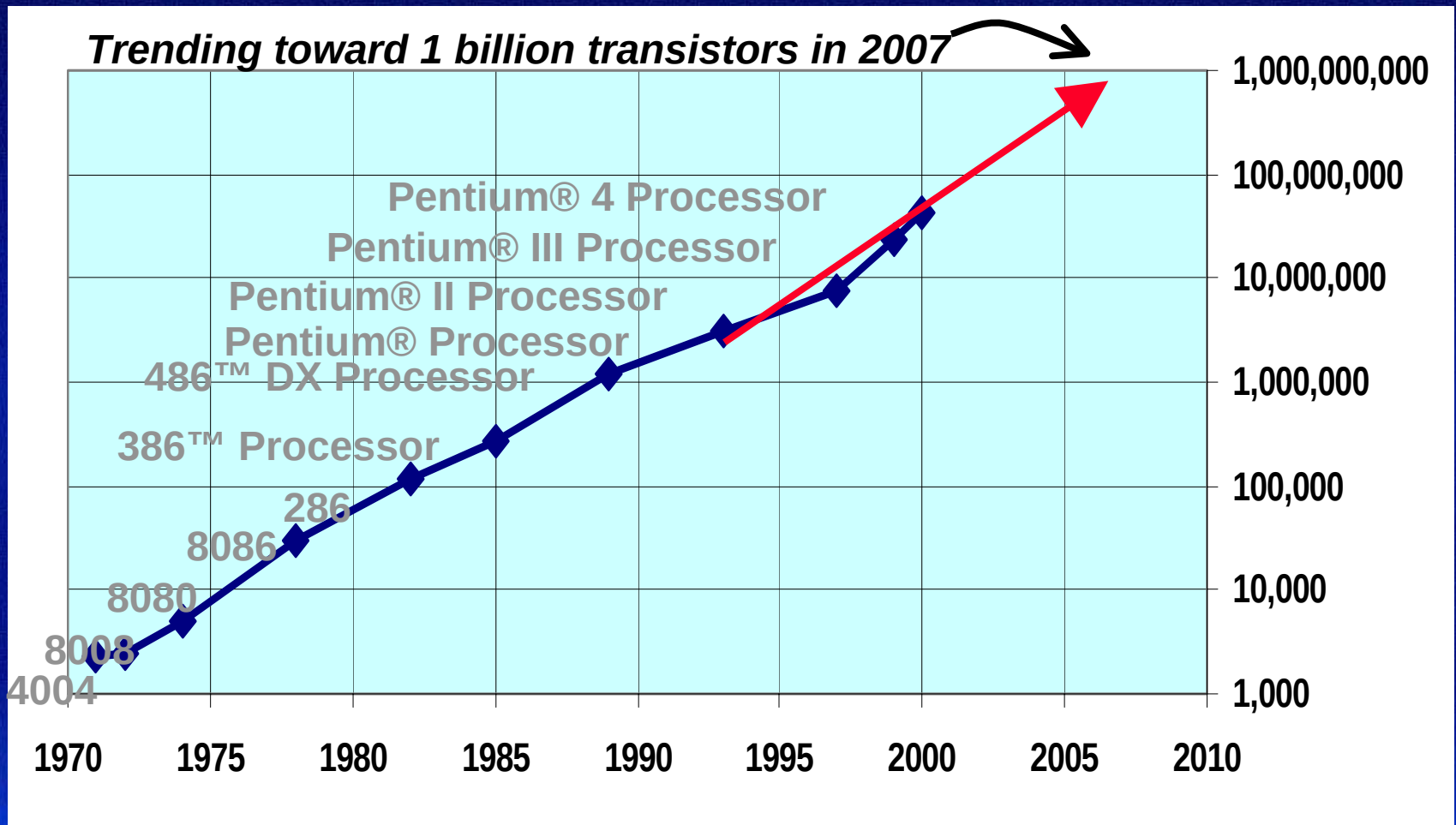
Outline

- Introduction
  - Trends
- Transistor / feature scaling challenge
  - Performance/power
- 2-D feature resolution and control challenge
  - Performance/density/cost
- Complexity/cost challenge
- Conclusion

Moore's Law Continues

Transistors doubling every 2 years toward the billion-transistor microprocessor



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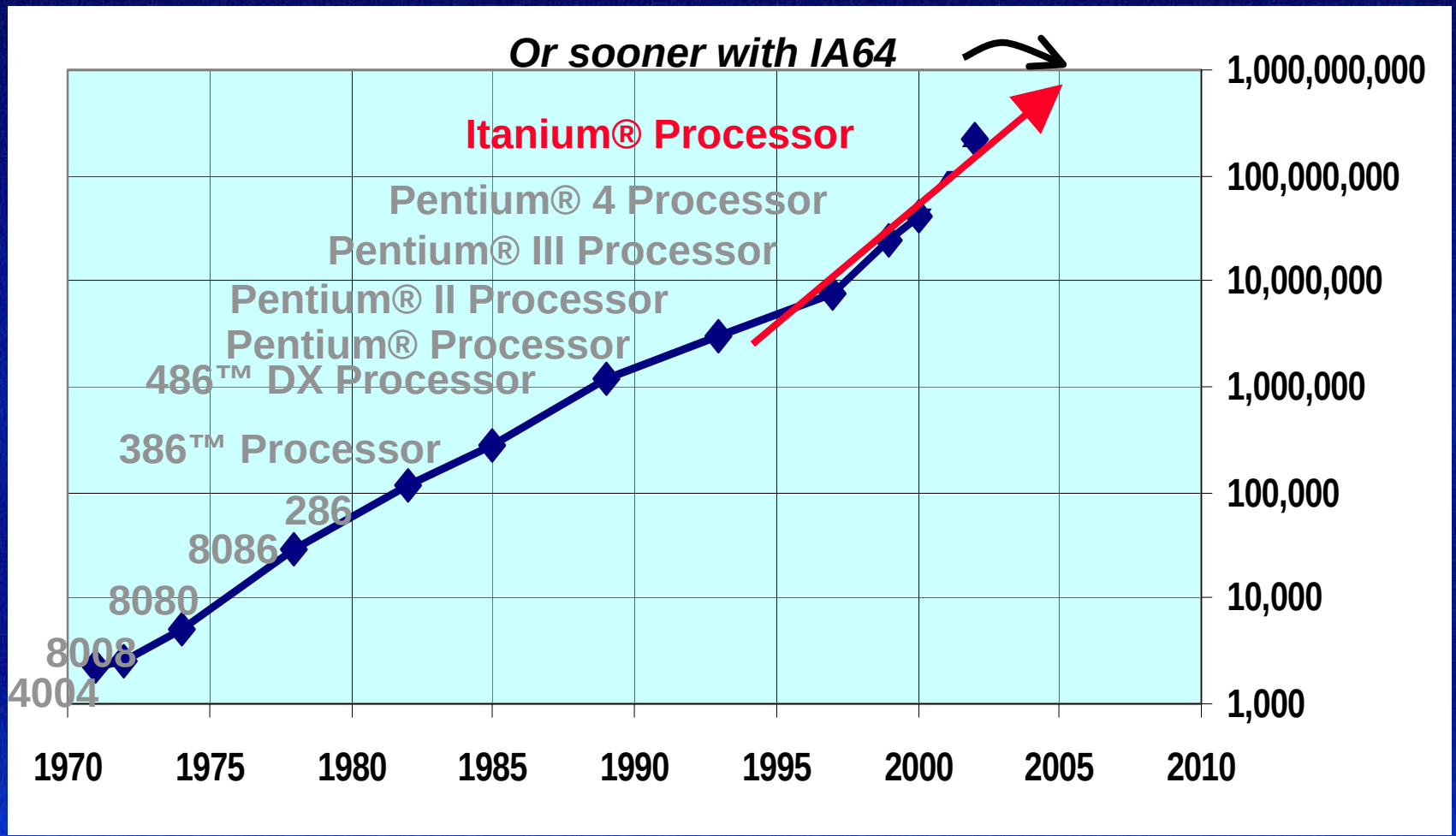

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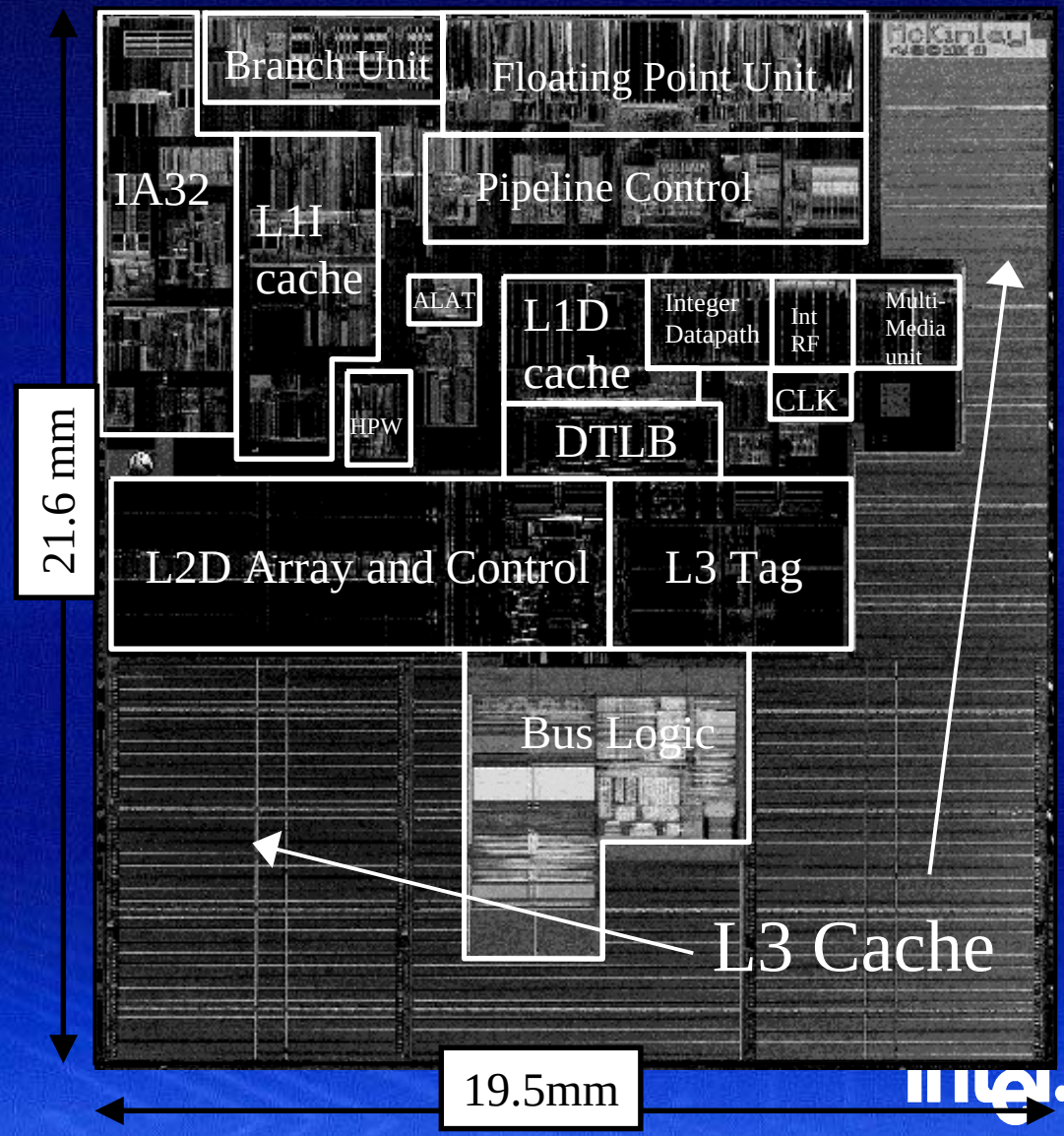
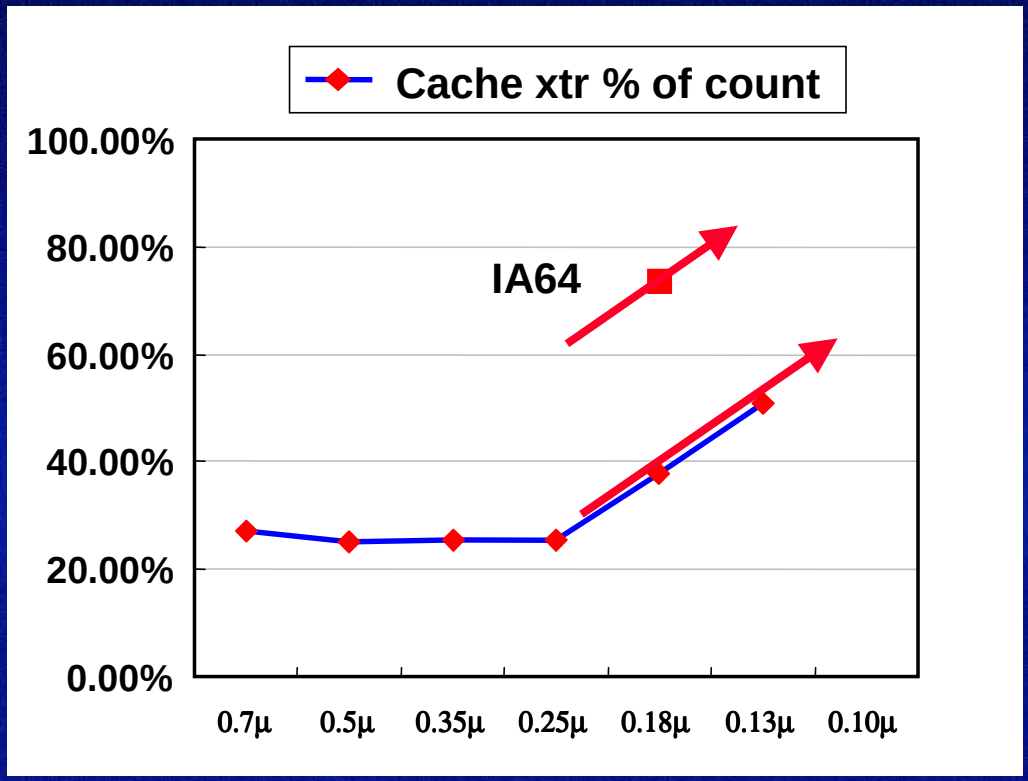
Itanium® Processor Overview

ISSCC 2002

- .18μm bulk, 6 layer Al process
- 8 stage, fully stalled in-order pipeline
- Symmetric six integer-issue design
- IA32 execution engine integrated
- 3 levels of cache on-die totaling **3.3MB**
- **221 Million total transistors**
- 130W @1GHz, 1.5V



On Die Cache Memory Trends



- Increasing % of total transistor count for cache
- Benefiting performance and power
- Increasing importance of optimized cache

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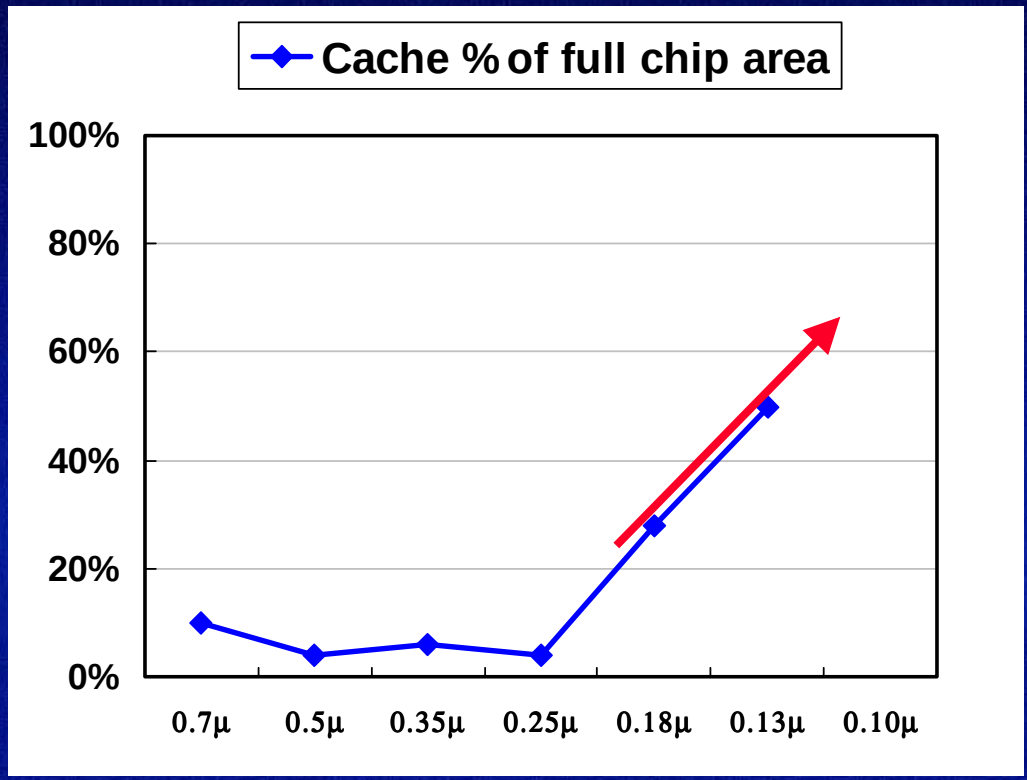
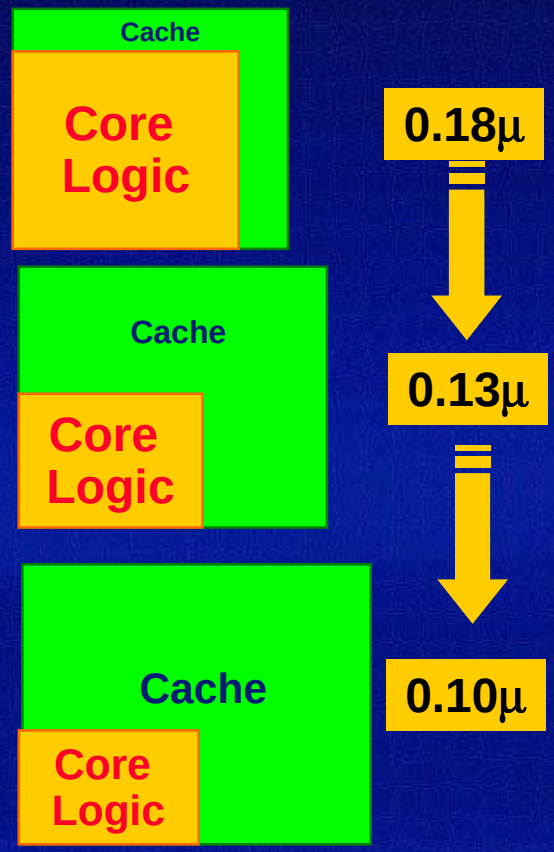
On Die Cache Memory Trends





Memory % of die area growing

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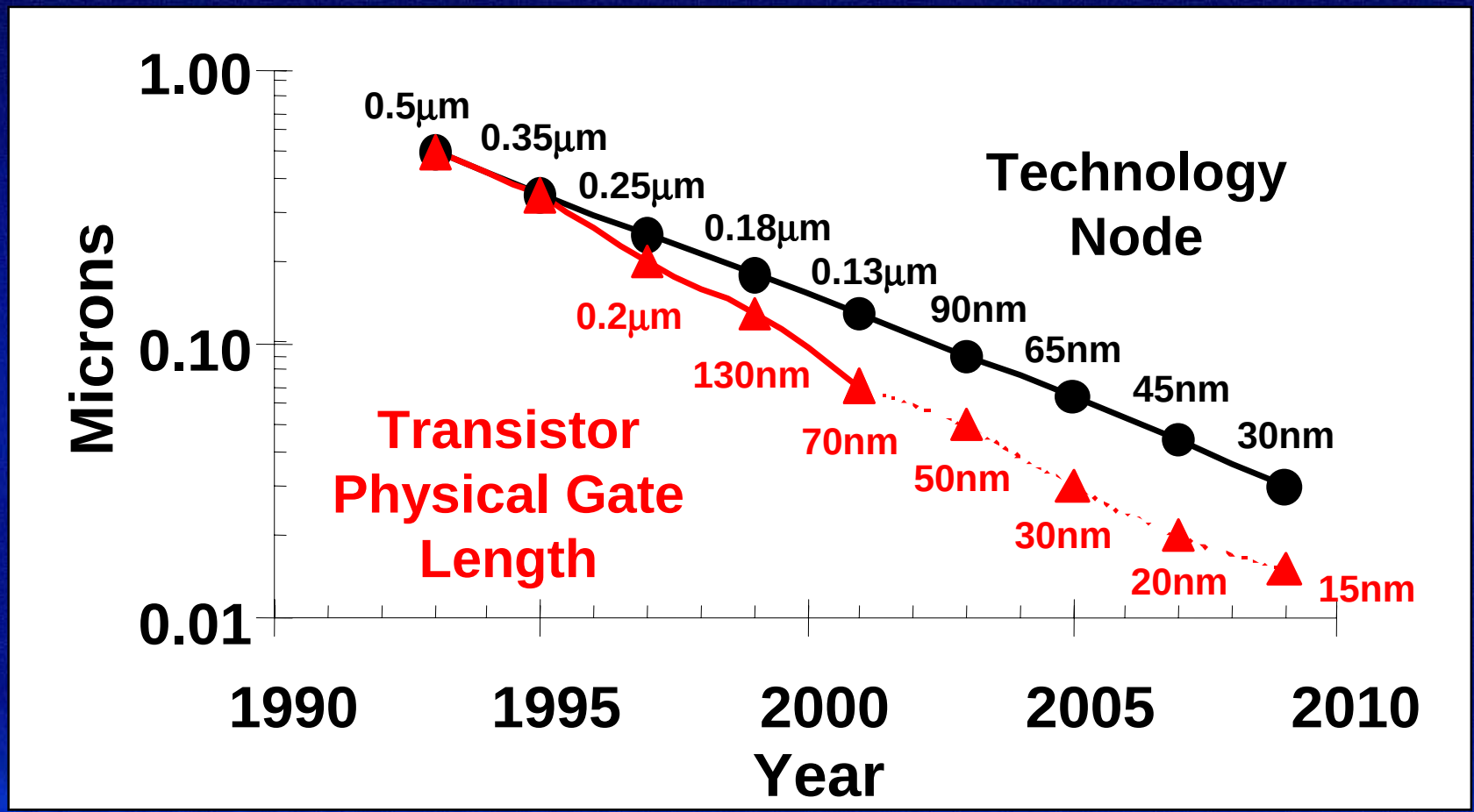
Transistor Physical Gate Length Trend (Lithography generation > L_{GATE})



Facilitated by 248, 193, 157, EUV lithography evolution

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Transistor progress has accelerated…

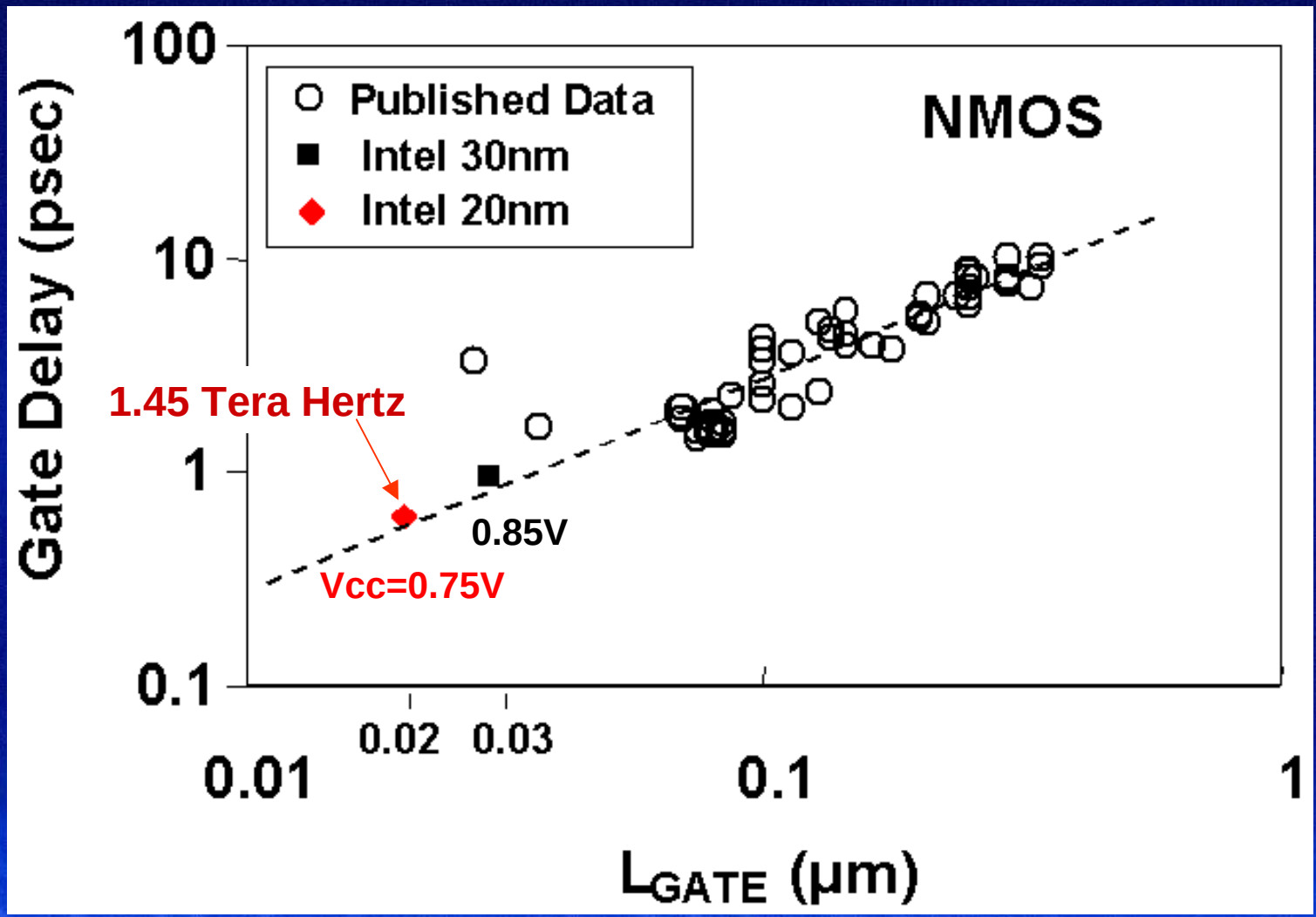
IEDM: December 2000

- 30nm gate CMOS; 0.8 nm oxides
- 1.2 THz at 0.85V
- Acceptable short-channel effects, junction leakage and gate leakage.

Silicon Nanotechnology Conference: June 2001

- 20nm gate NMOS
- 1.45 THz at 0.75V

Intel Has Demonstrated the World's Fastest and smallest Transistors



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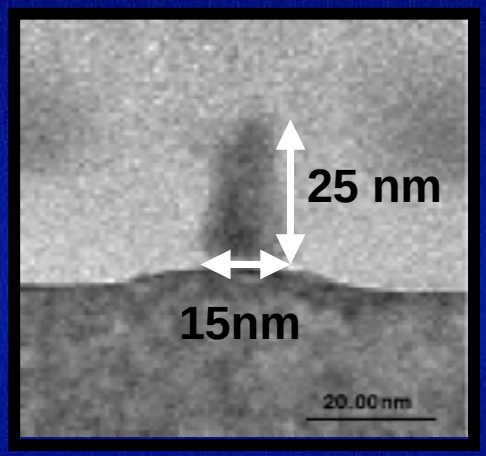
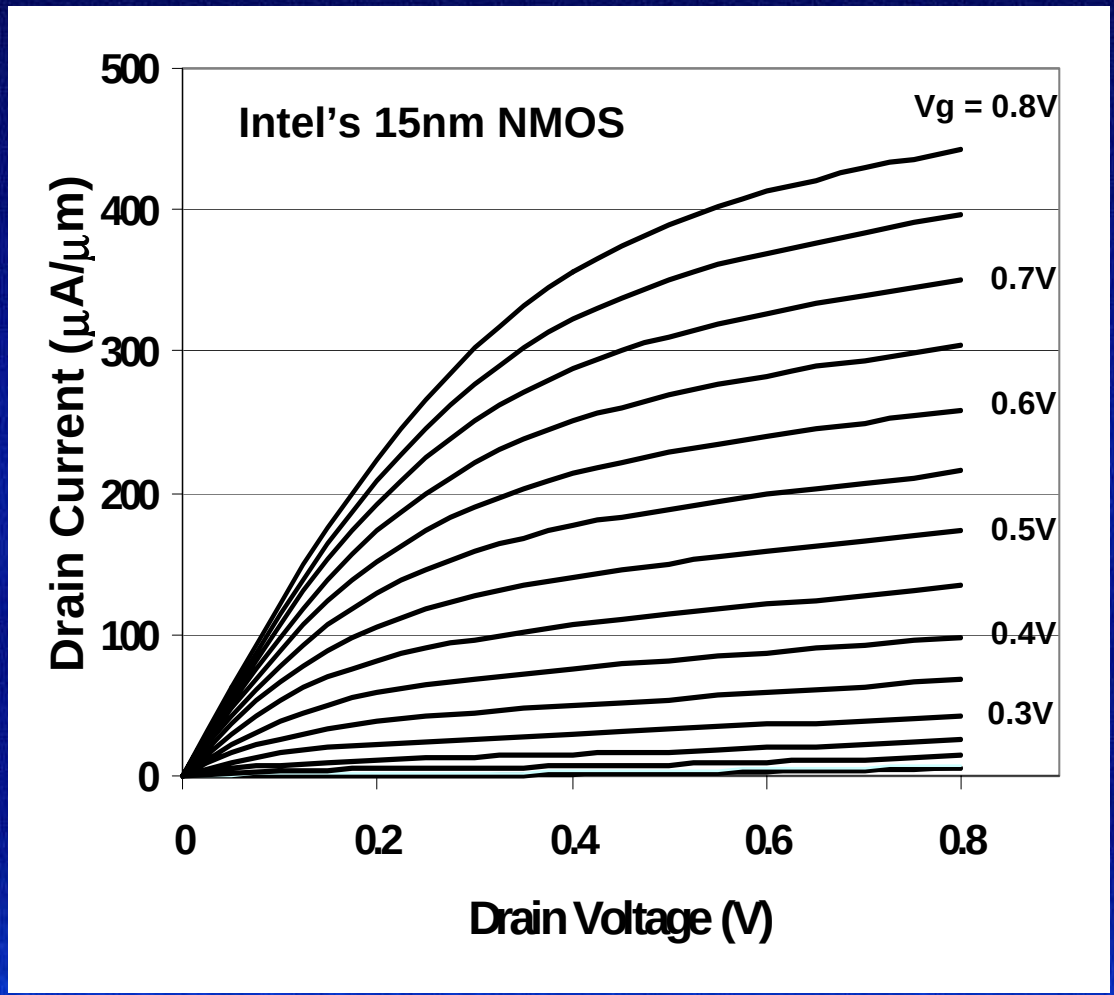
Intel's 15nm NMOS Transistor

Significant new capability demonstration





2.63 THz gate delay @ 0.8V

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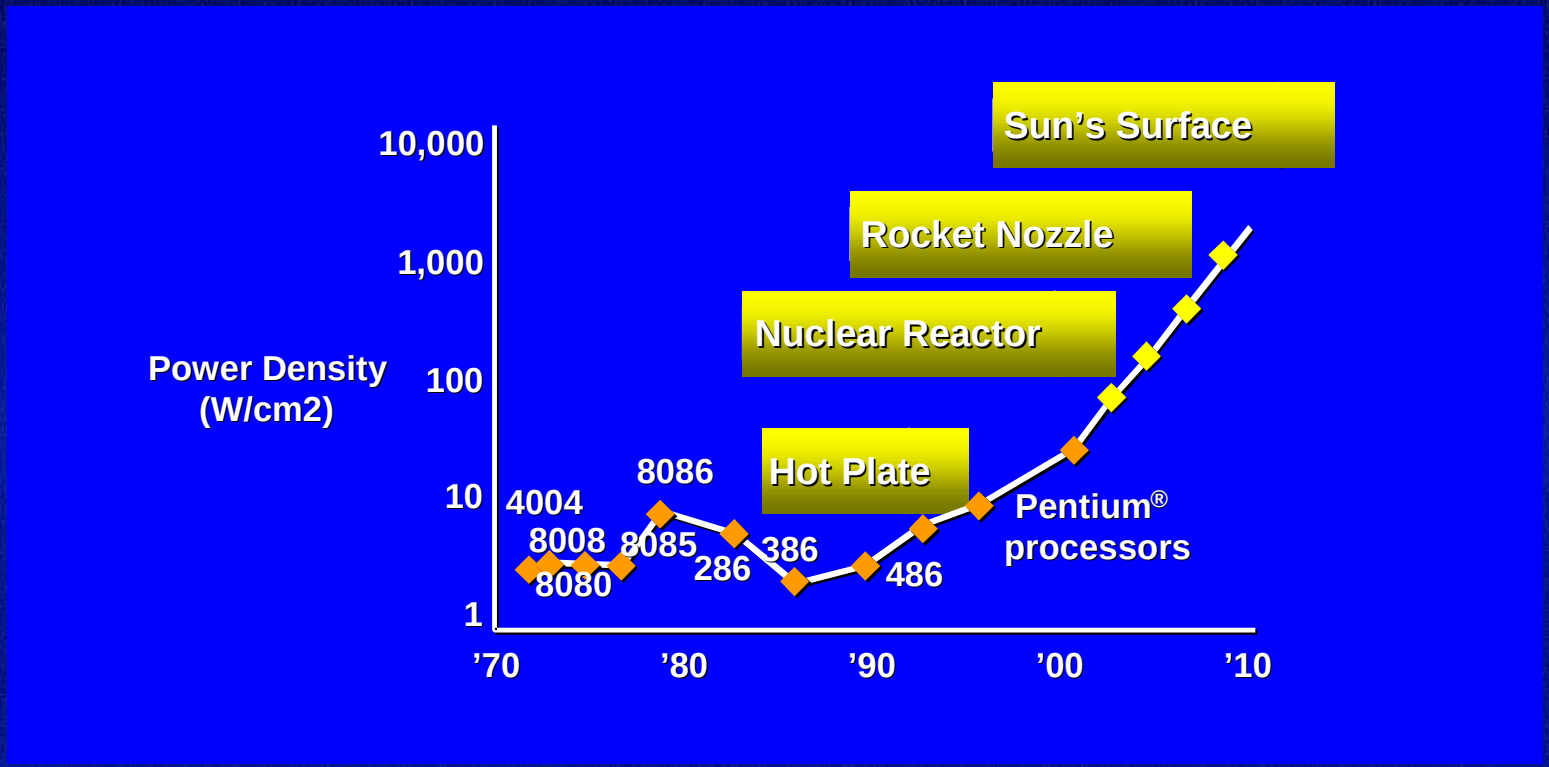
The Power Challenge:

- Power consumption starting to rise exponentially
- Driven by:
  - Transistor I_{OFF} Leakage
  - Transistor Gate Leakage
  - High Operating Voltage

Power Density Extrapolation



Pat Gelsinger's Slide from ISSCC 2001

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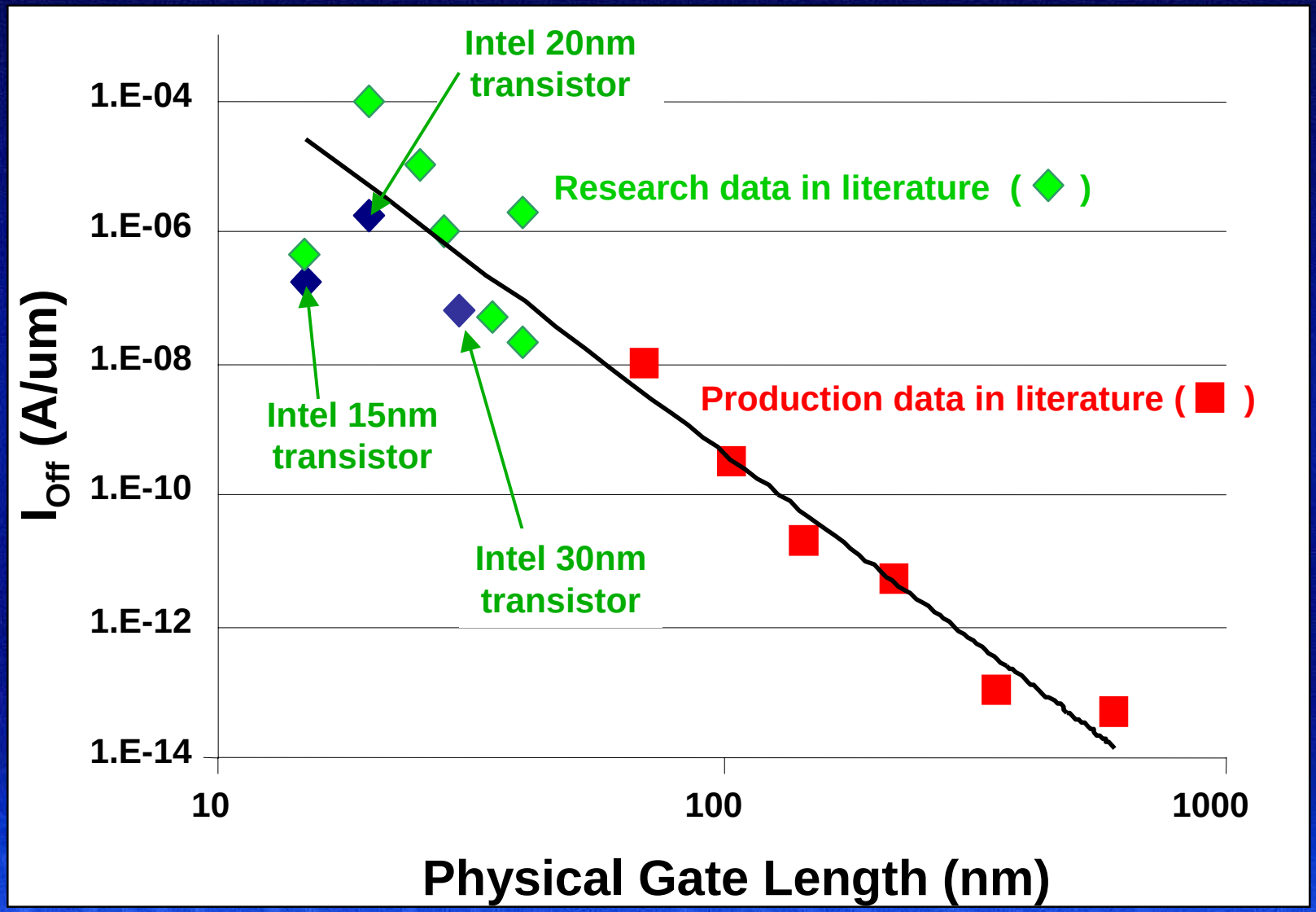
Transistor I_{OFF} Leakage Growing



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Fundamental Challenge for This Decade

- Continue Moore's Law without Exponential increase in Power Consumption
  - 30% Delay scaling
  - 50% area reduction
- Intel introduced two important technologies at IEDM :
  - Depleted substrate transistors
  - High K gate dielectric
- Our long term approach is:
  - TeraHertz Transistors

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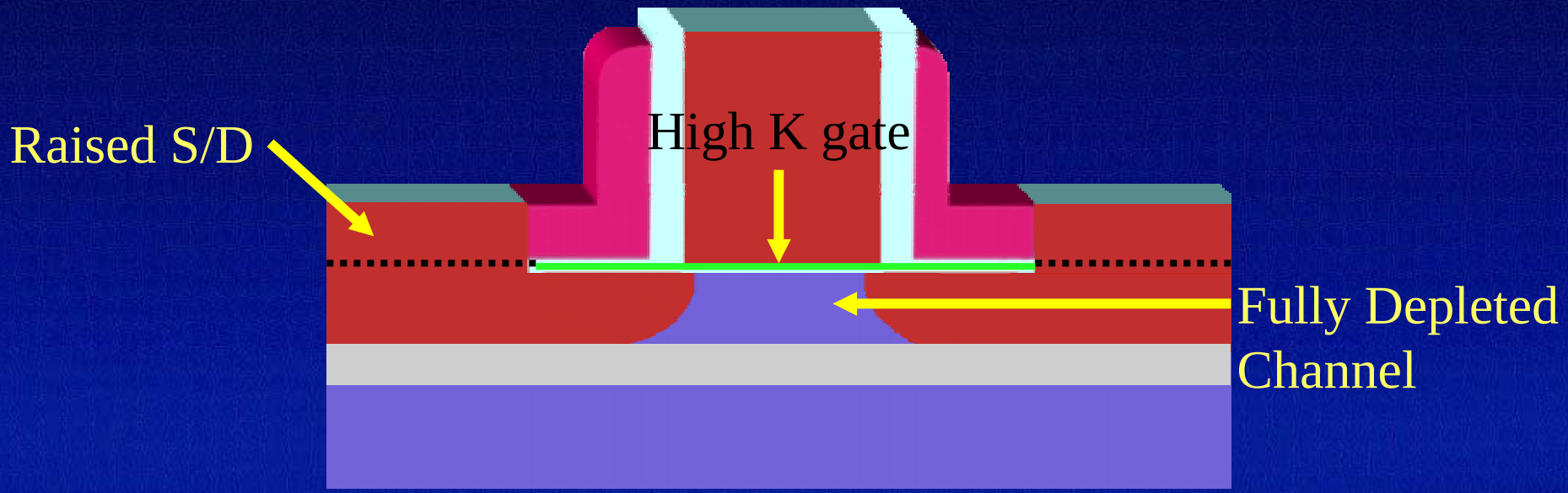
Solutions

TeraHertz Transistors
Intel's New Transistor Architecture

- Depleted Substrate Transistor (DST)
  With Raised source and drain
- High-K gate dielectrics
- Low voltage operation

TeraHertz Transistor Architecture



- Eliminates subsurface leakage
- Solves high resistance
- Minimizes gate leakage
- Eliminates floating body effect
- Minimizes soft error rates
- 50% lower junction capacitance that PD SOI

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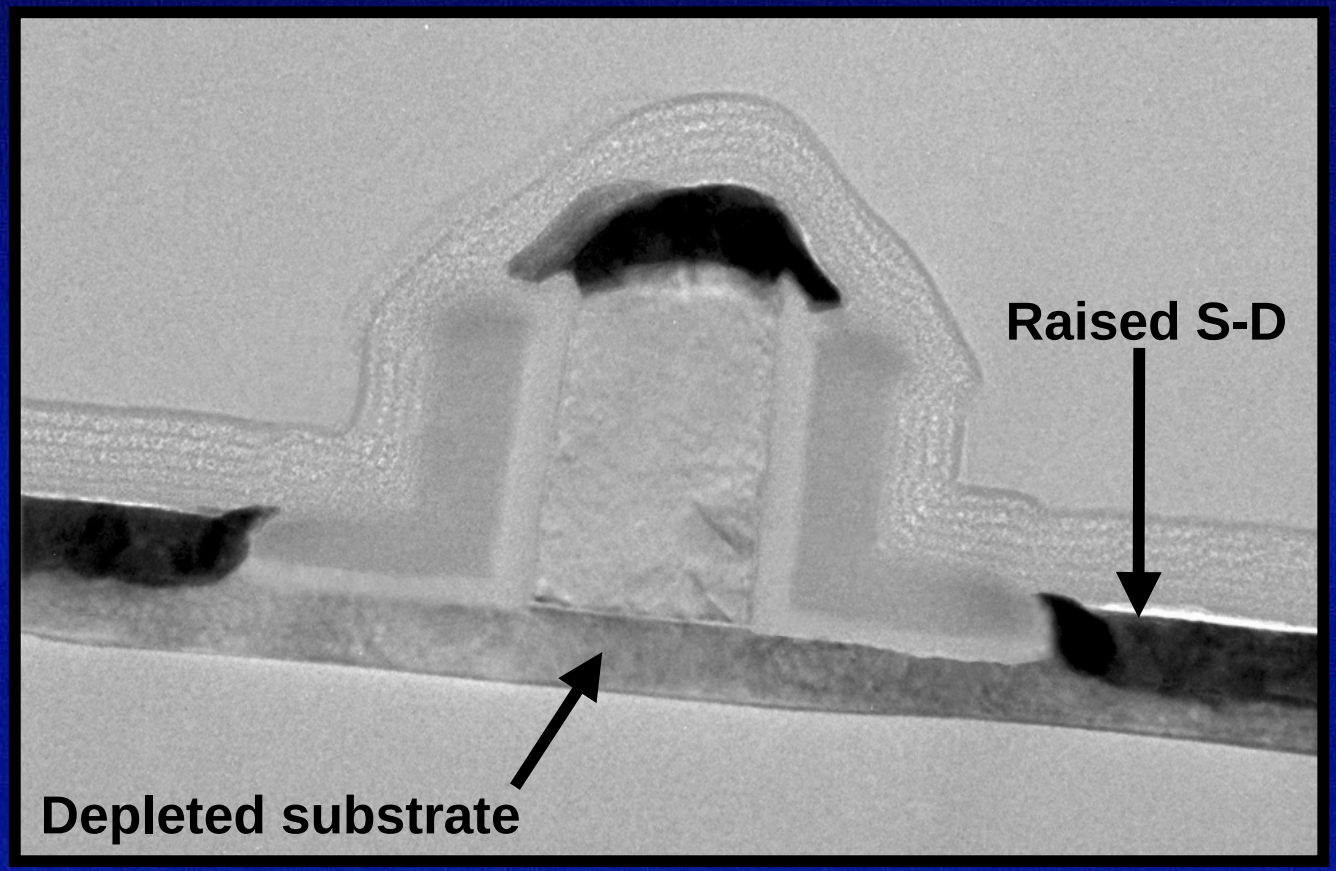
Raised Source-Drains Combined with Depleted Substrate



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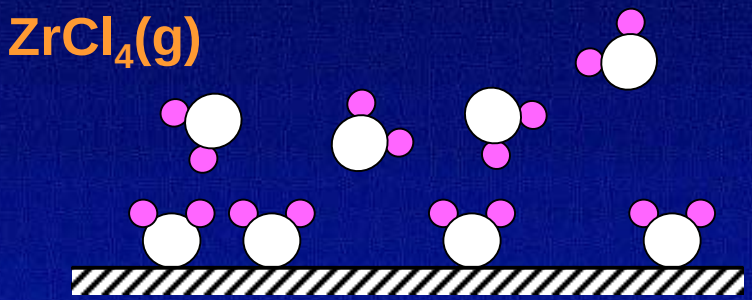
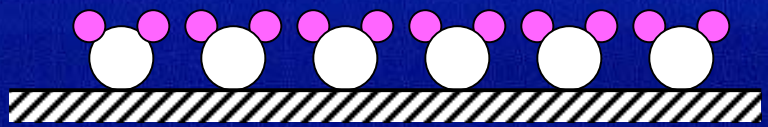
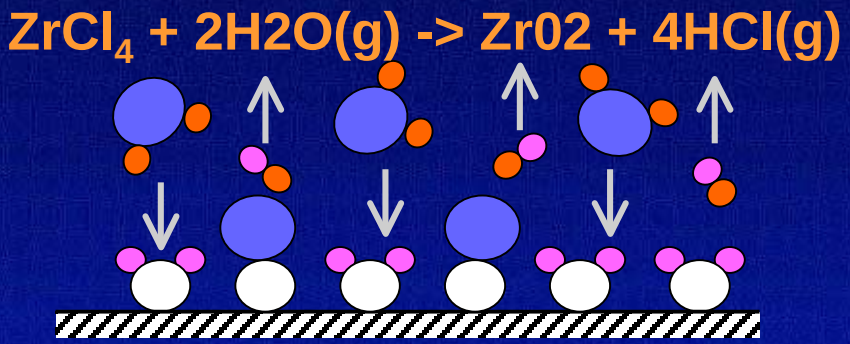
High-K Gate Dielectric Formed Using Atomic Layer Deposition



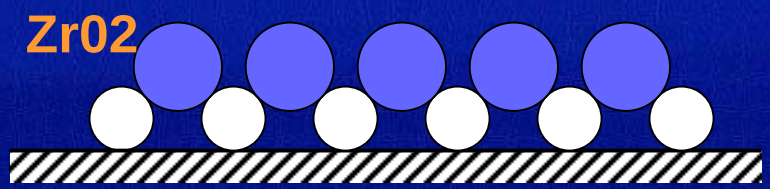
Step 1



Step 2



Step 3



Step 4

- Sequential introduction of precursors ZrCl4(g), H2O(g)
- Surface reaction between substrate & each precursor until saturation

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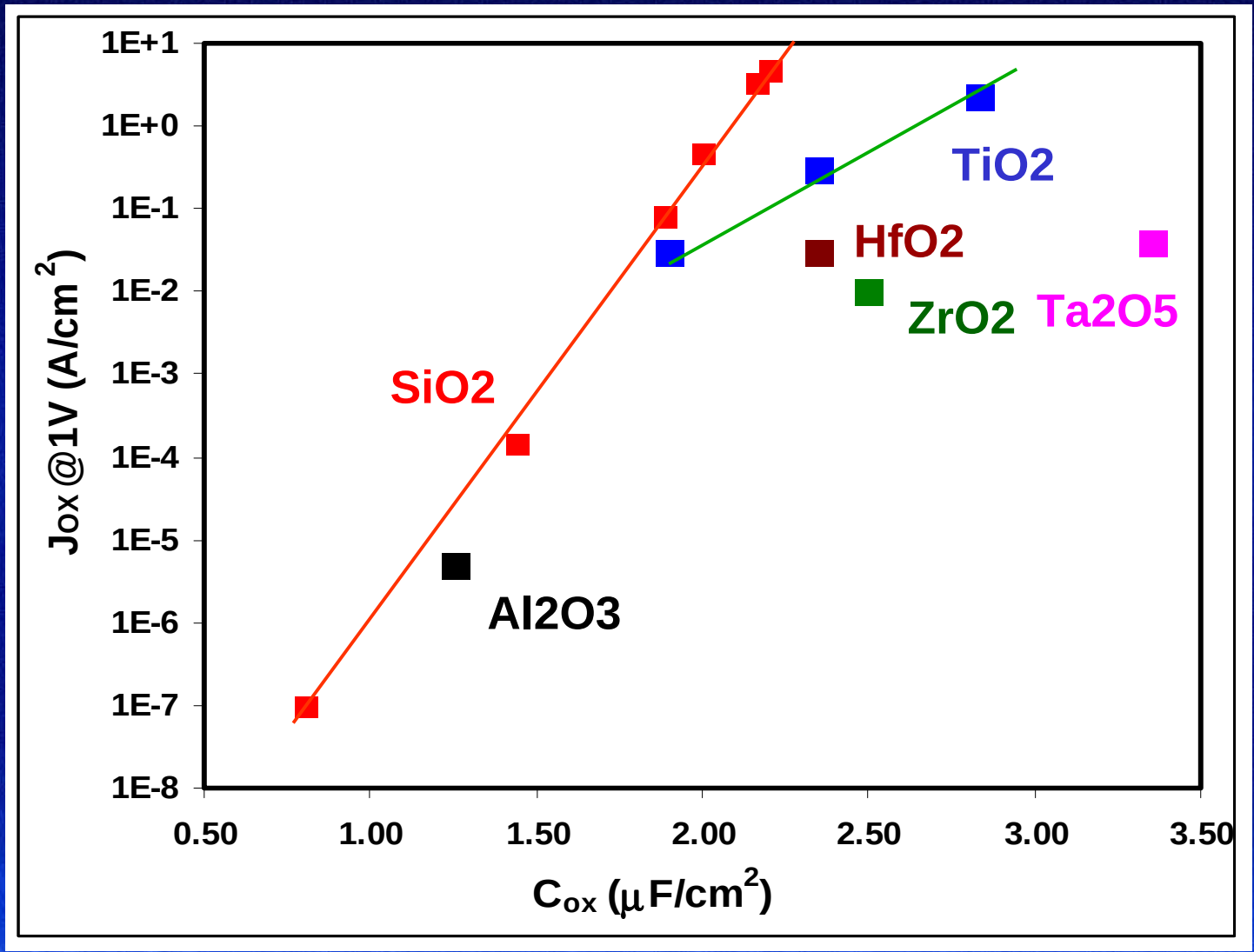
Alternative Gate Dielectrics to Reduce Gate Leakage



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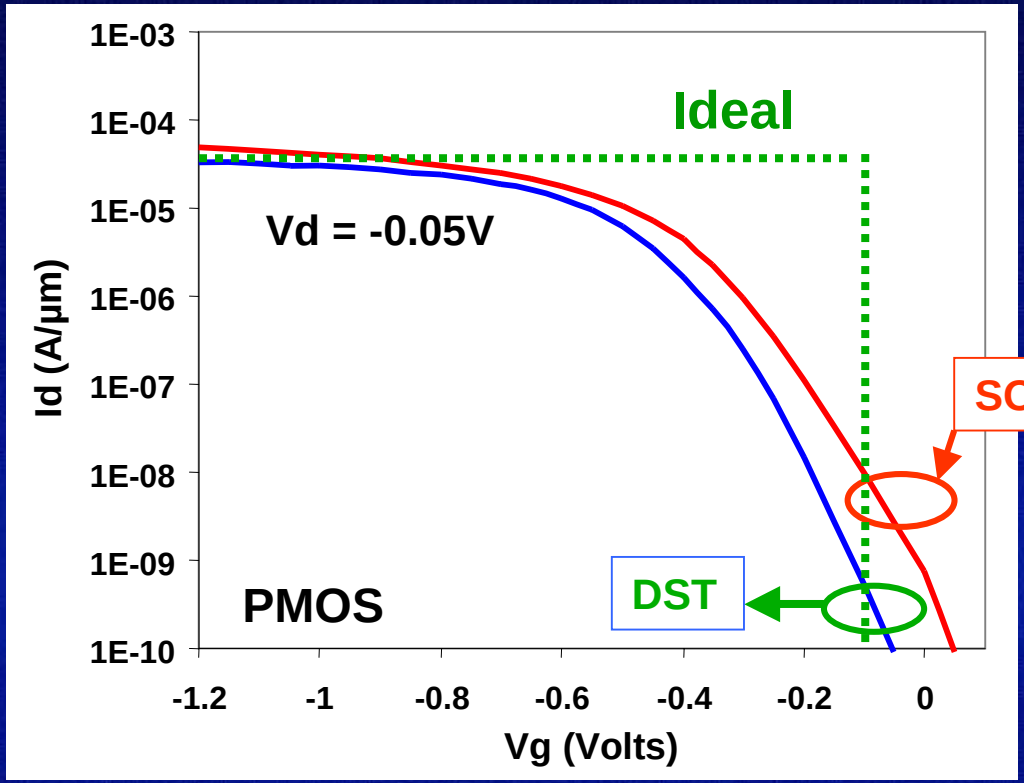
DST Outperforms PD SOI



- DST achieves much steeper sub-threshold slope and lower I_{off} than both SOI and bulk Si
- Up to 100x lower leakage than partially depleted SOI !

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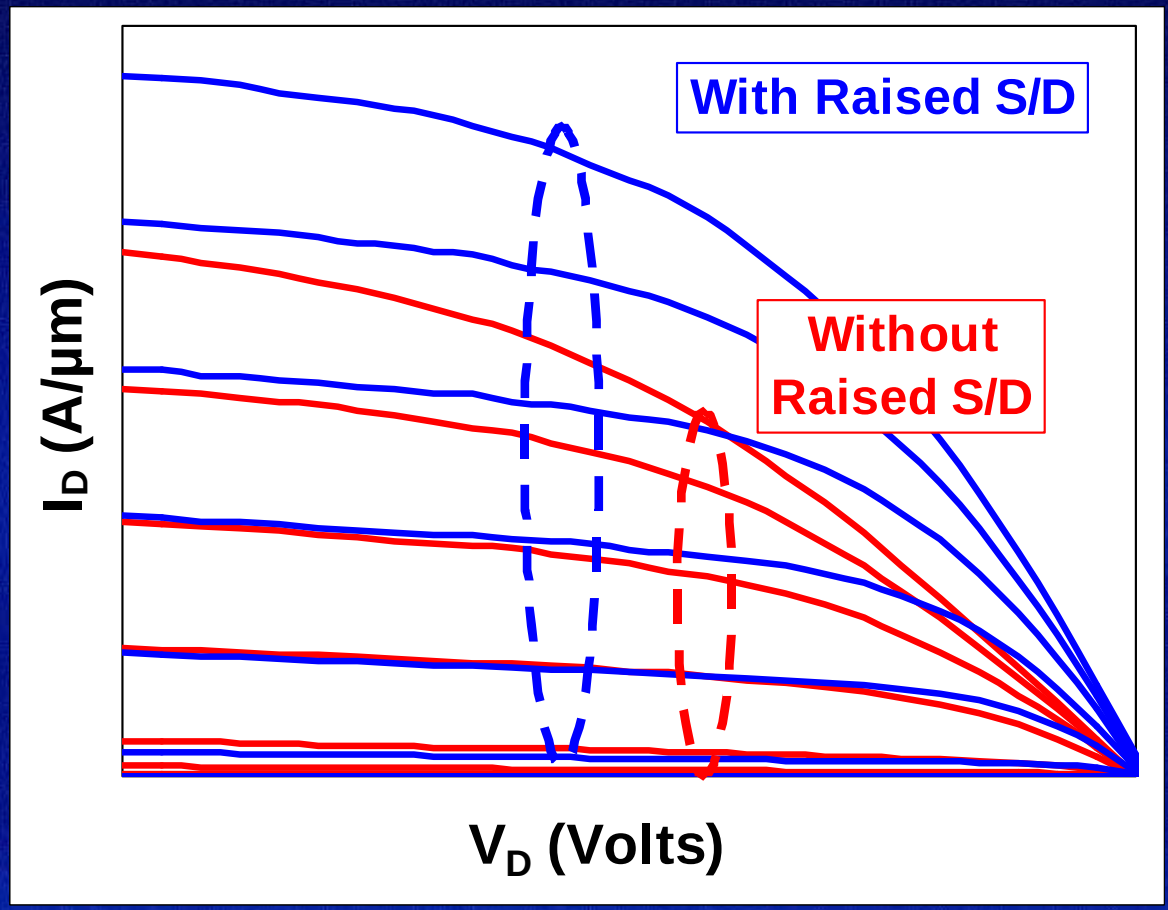
Raised Source and Drain Reduces Parasitic Resistances and Improves IDSAT



30% increase in drive current!

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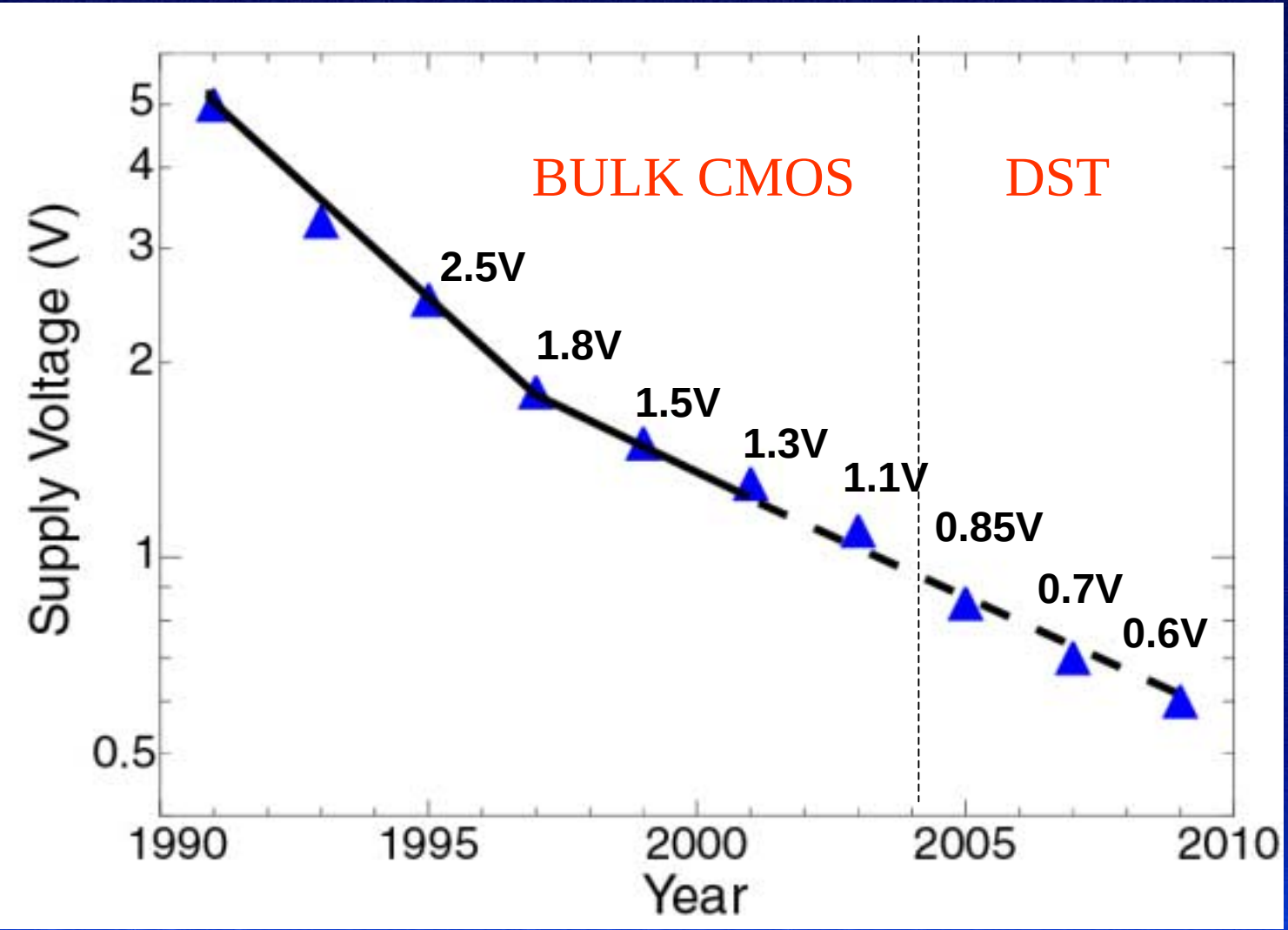
DST Enables Future Voltage Scaling



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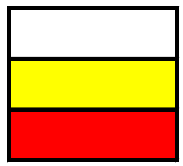
ITRS Lithography Control Challenge

Year Of Production	2001	2002	2003	2004	2005	2006	2007
MPU 1/2 Pitch (nm)	150	130	107	90	80	70	65.00
MPU gate post etch (nm)	65	53	45	37	32	28	25.00
Gate control (3 sig) (nm)	5.3	4.3	3.7	3	2.6	2.4	2.00

Solutions exist, are being optimized
Solutions are Known
Solutions NOT known



- Control solutions need to be found
- Impact of control issue: performance loss

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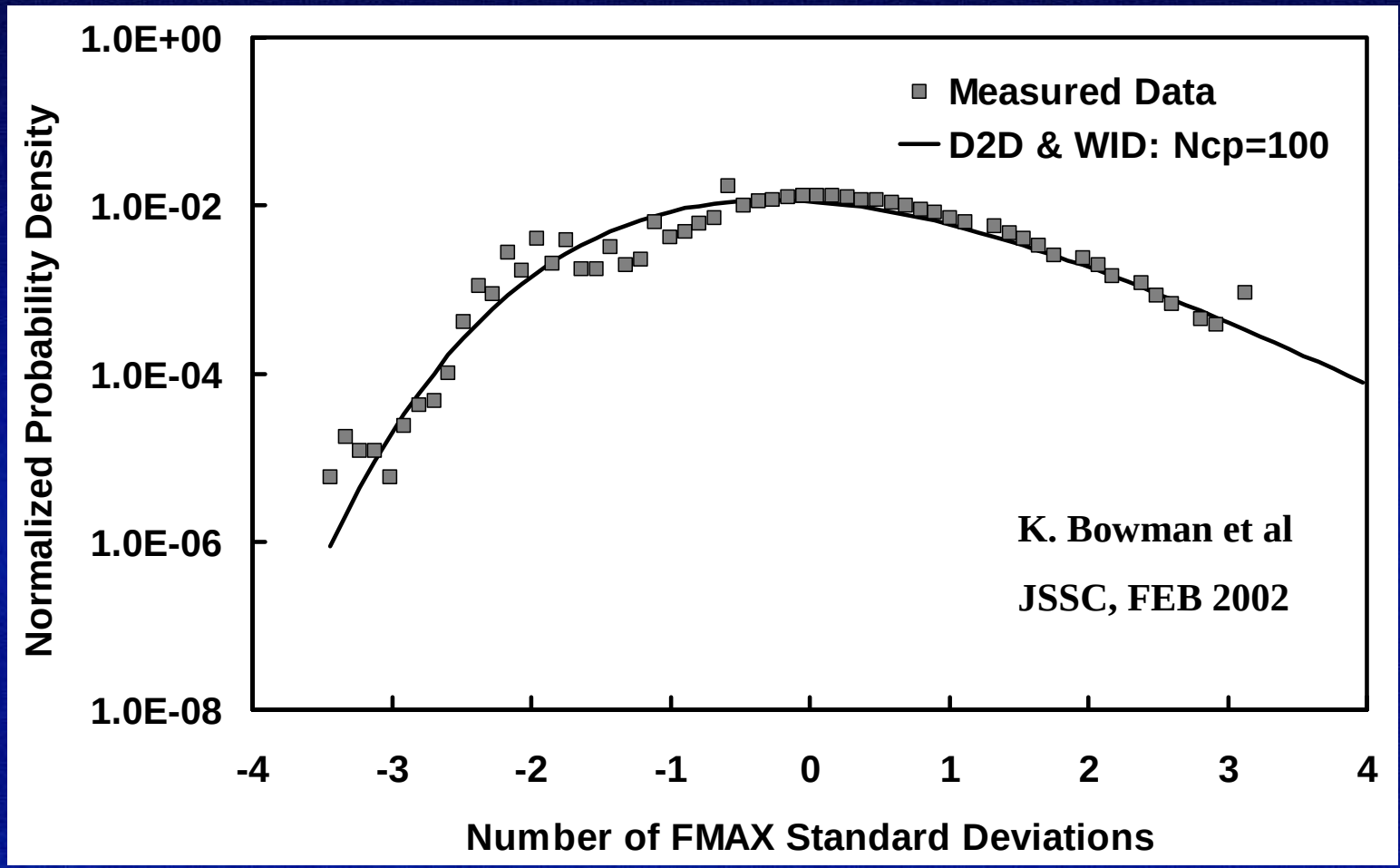
FMAX Vs Variation Model Established



- Model agrees closely with measured data for a 0.25 μm microprocessor in *mean*, *variance* and *shape*
- *Model can be used to project future variance impact*

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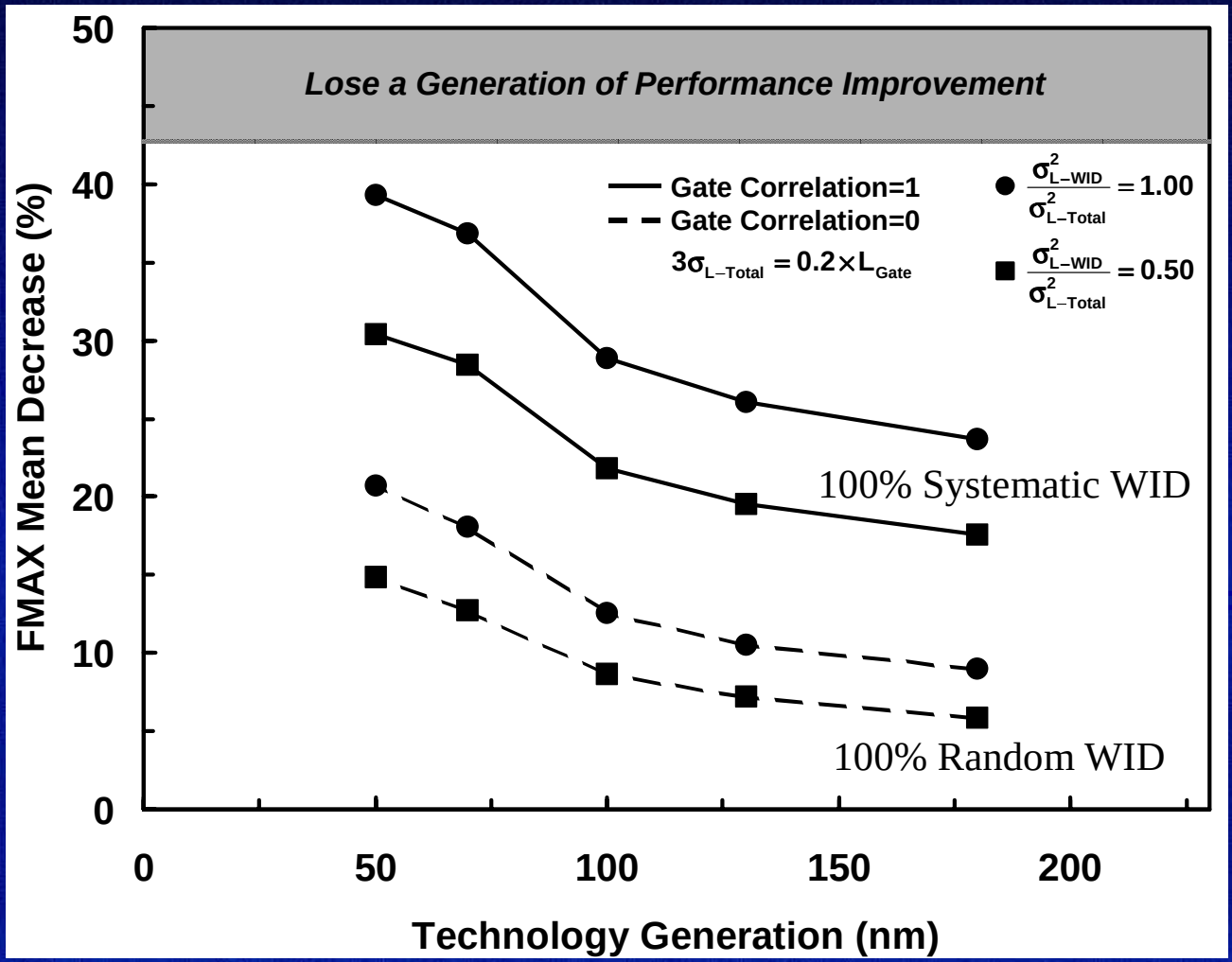
Projecting the Impact of *Within-Die Variation*



Reduction in Gate Delay per Generation

$\%T_D$ Decrease $\approx 30\%$

$\%F_{CLK}$ Increase $\approx 43\%$

F_{CLK} Improvement Resulting from Transistor Scaling

- ***Essentially a generation of performance gain can be lost due to systematic within-die fluctuations at the 50 nm technology node***
- ***Suggests control must hit or improve on ITRS goals***

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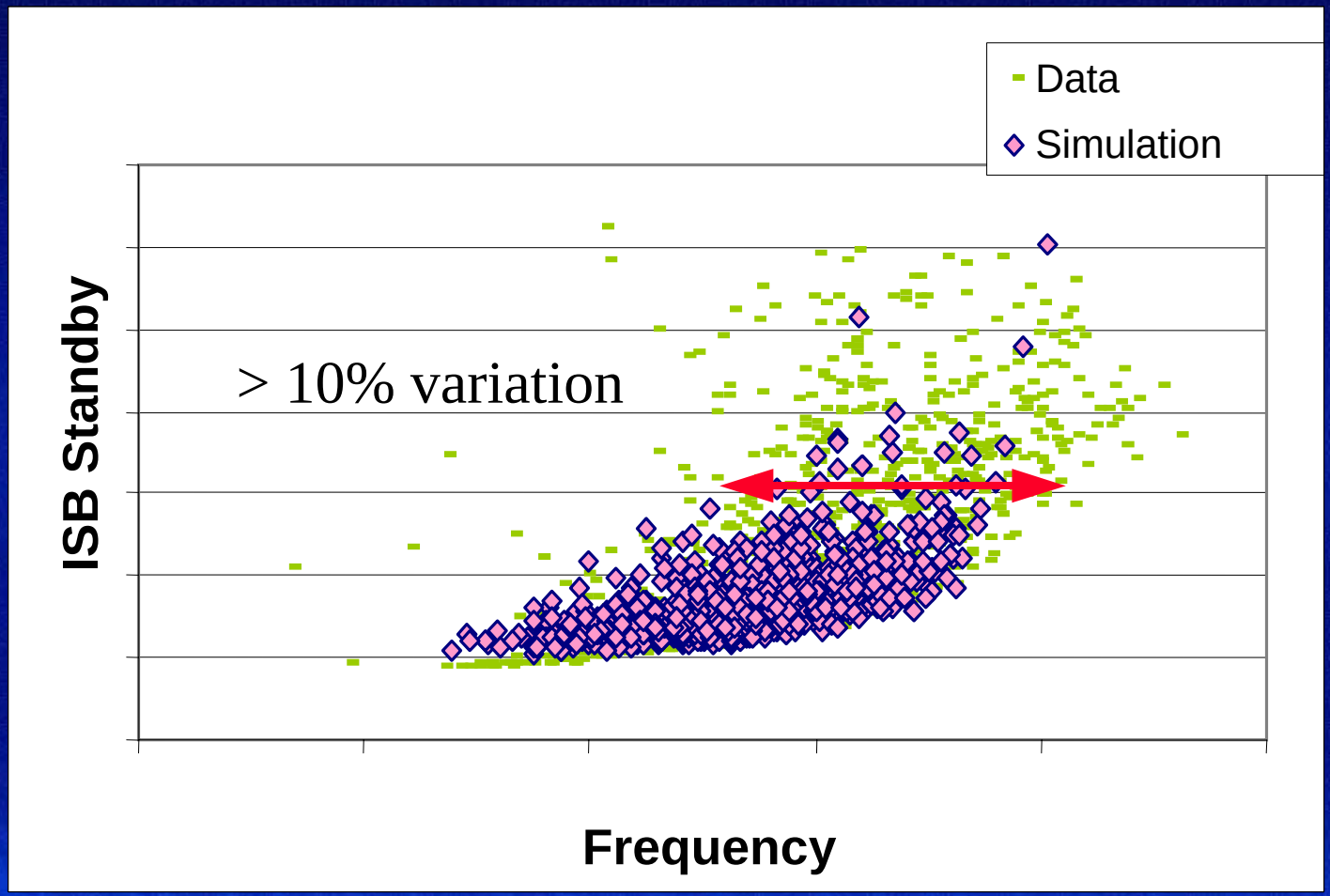
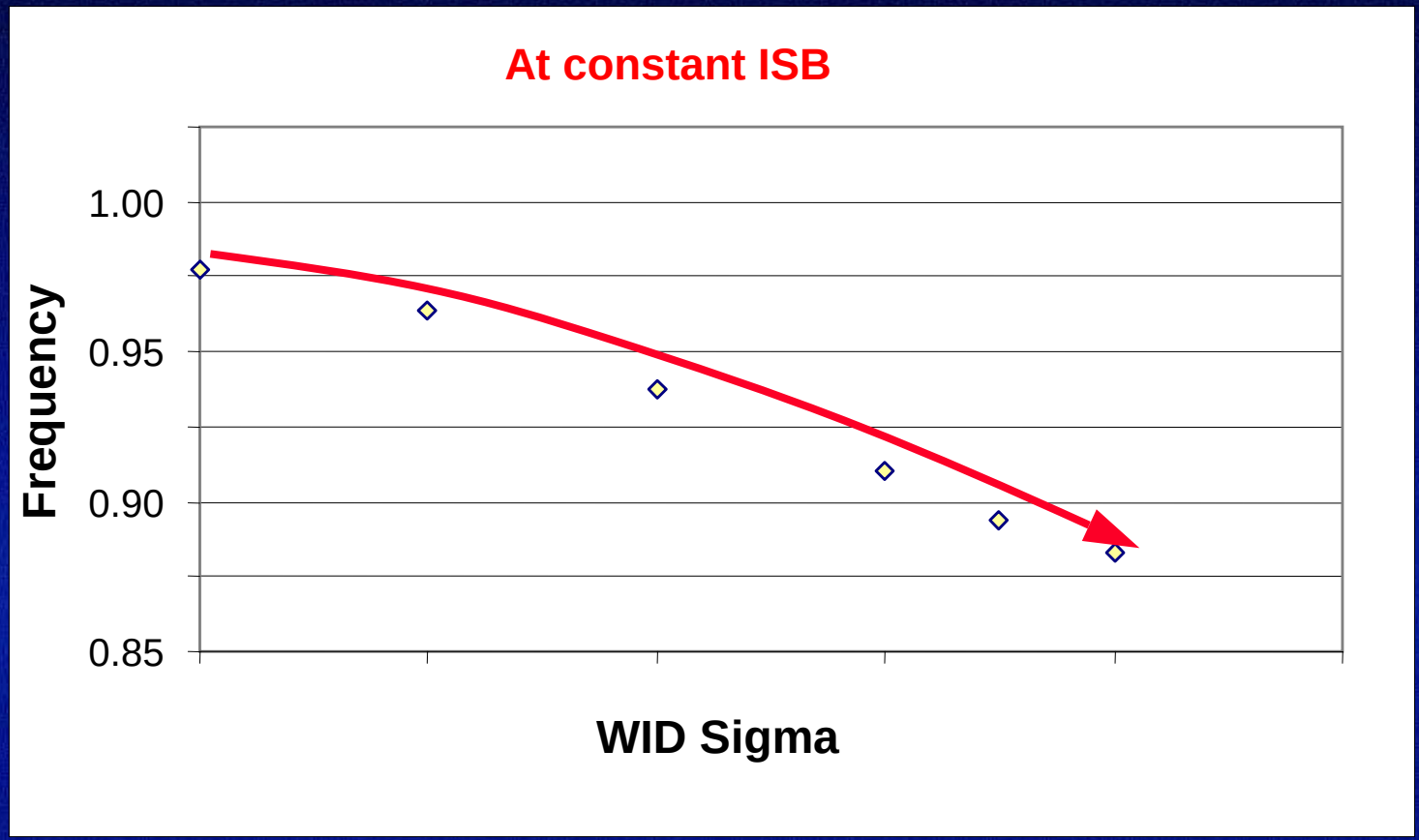
Fmax vs Isb Model



Model illustrates impact of variation: DTD,WID, device

Modeled FMAX Vs WID



- **WID variation impacts Mean FMAX Vs ISB significantly: ~ *10% impact.***

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Strategies To Address Variation

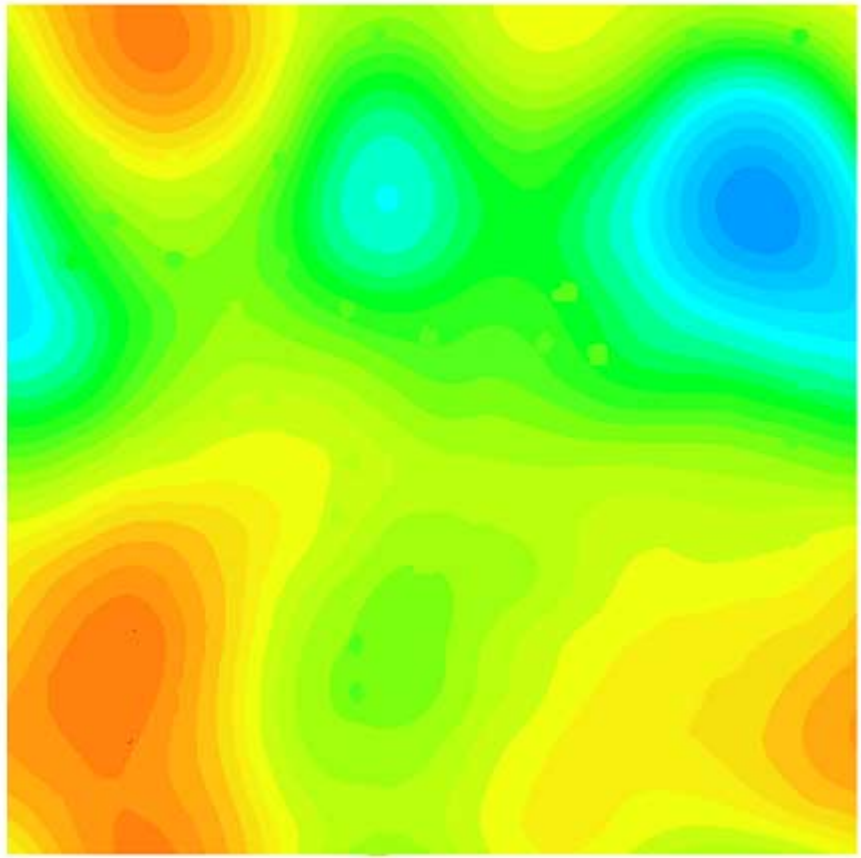
Potential design approaches:

- **More compensation circuitry:**
  - **Clock, logic, etc**
  - **Adds area, complexity ⇒ cost**
- **Reduce degrees of freedom:**
  - **Orientation, pitch constraints, random layout elimination, more simplified array like structures**
  - **Likely area impact ⇒ cost**
- **Improve design uniformity:**
  - **Design structures, better dummification**
  - **Added complexity**

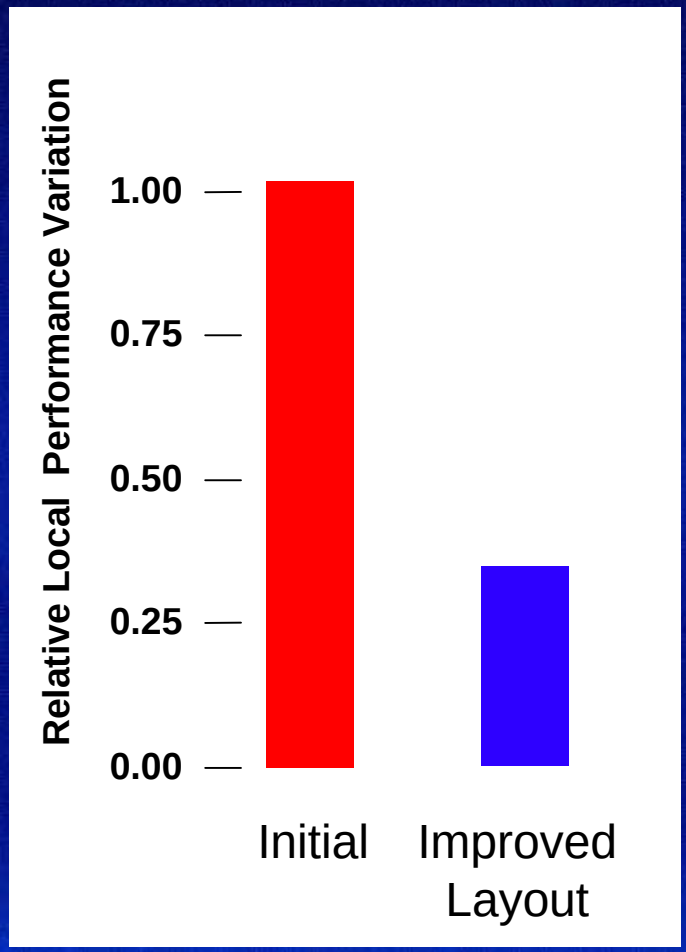
Cost / benefit optimization will be required

- **Will likely need to do most of the above**

Example: Local Performance variation Induced by Poly Density Variation



Initial modeled performance variation



Multiple sources: mask writing to poly etch

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Strategies To Address Variation

Potential technology approaches:

- **Improve the tools**
- **More advanced OPC, RET**
  - **Mean, sigma control**
- **Advanced Process Control**
  - **Requires good stable models, logistics/automation**
- **Custom corrected tools/reticles**
  - **Requires good stable models, logistics/automation**
- **Added process steps**

Cost / benefit optimization will be required

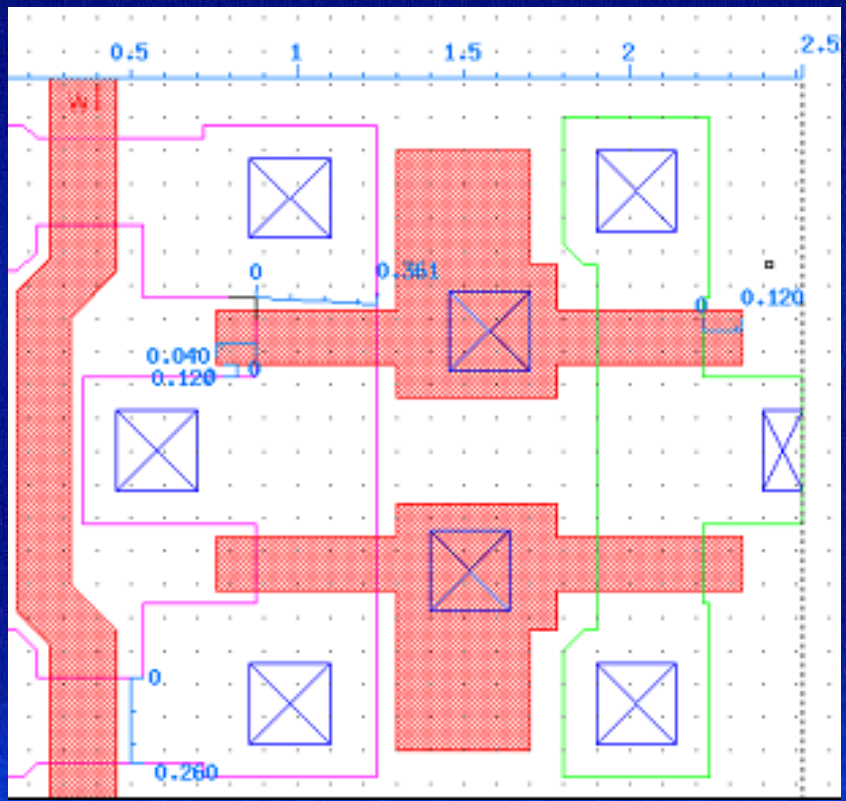
- **Will likely need to do most of the above**

Cache Strategies, 2D Effects

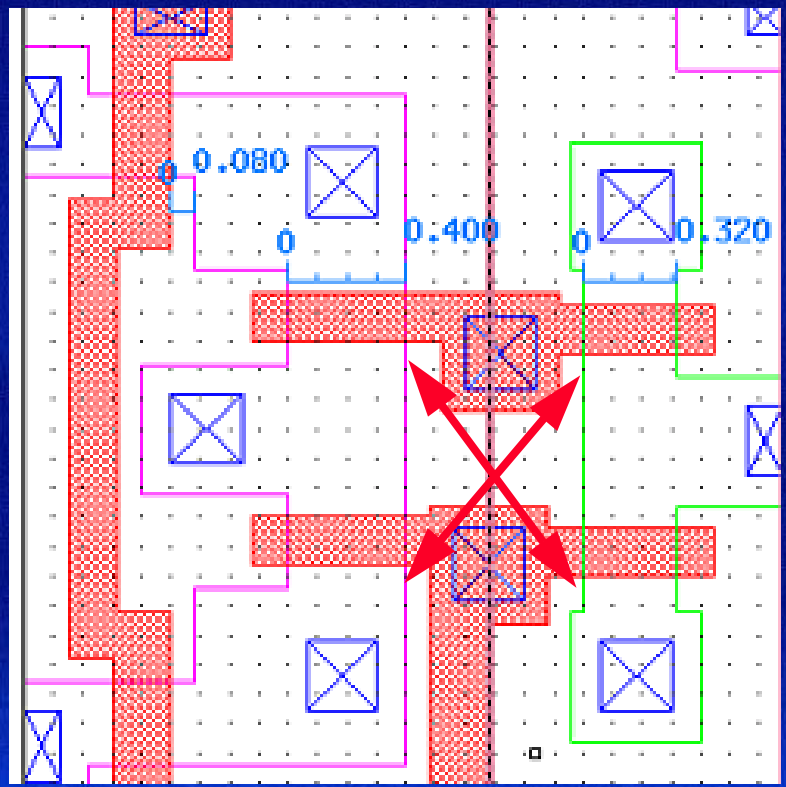
- **Growing cache sensitivity:**
  - **Cache arrays sensitive to cell stability**
  - **Dopant fluctuation, CD (Z/L) device variation**
  - **2D patterning effects significant in compact layout**
- **Cache specific optimizations:**
  - **Control of layout symmetry through modeling**
  - **Optimized design rules, cell size, array size**
  - **Optimized use of redundancy, ECC, VCC**
  - **All are potential cost factors**
- **With the growth of cache on die, careful cost / benefit analysis required**

Role of Symmetry

Symmetric reference



Asymmetry between P/N transistors pairs.



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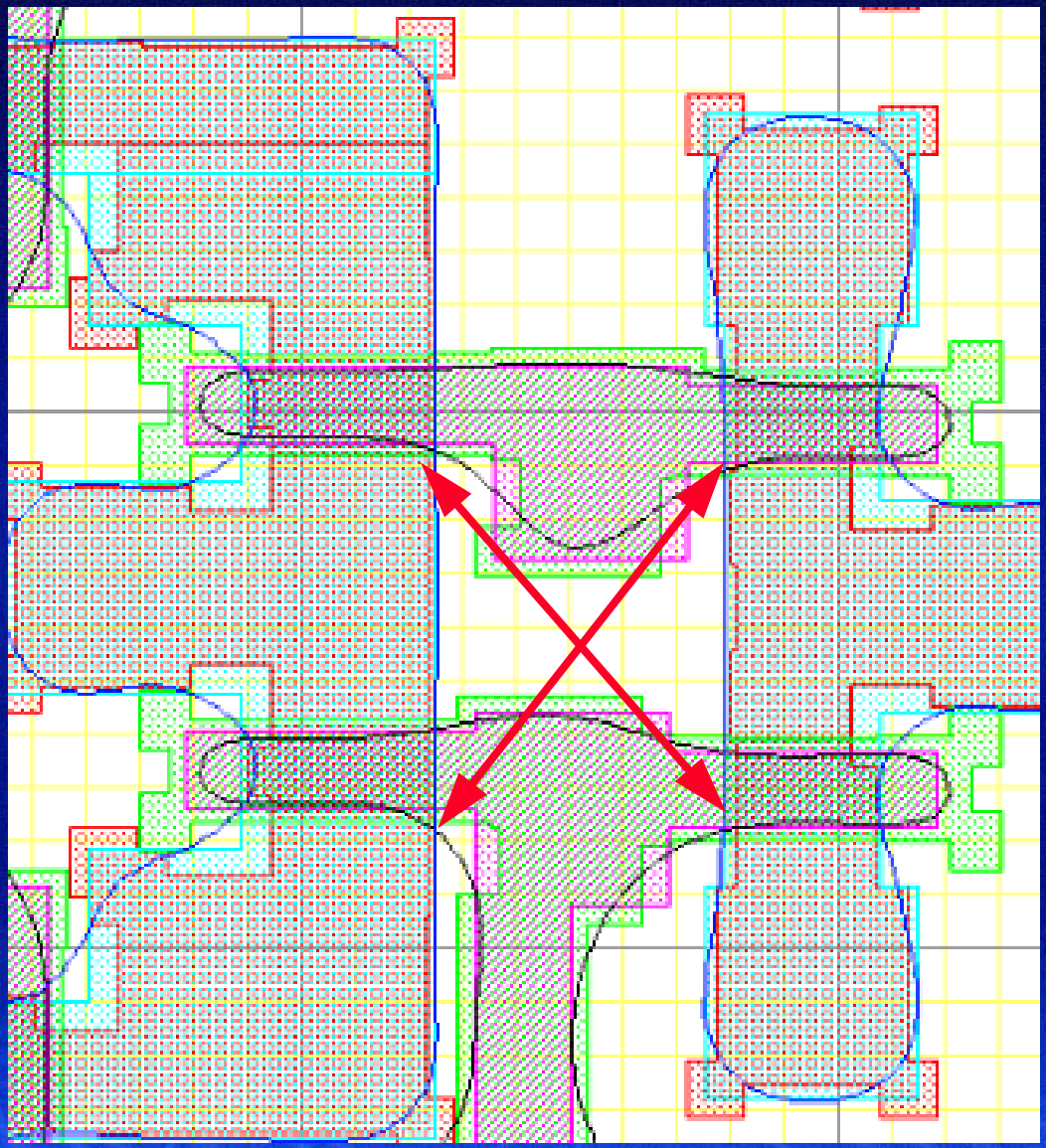
Role of Symmetry: Analysis Through Simulation



Asymmetry in P/N cross coupled device Z/L impacts cell balance

Cell stability degraded ~ 100x

Modeling required to confirm acceptable layout

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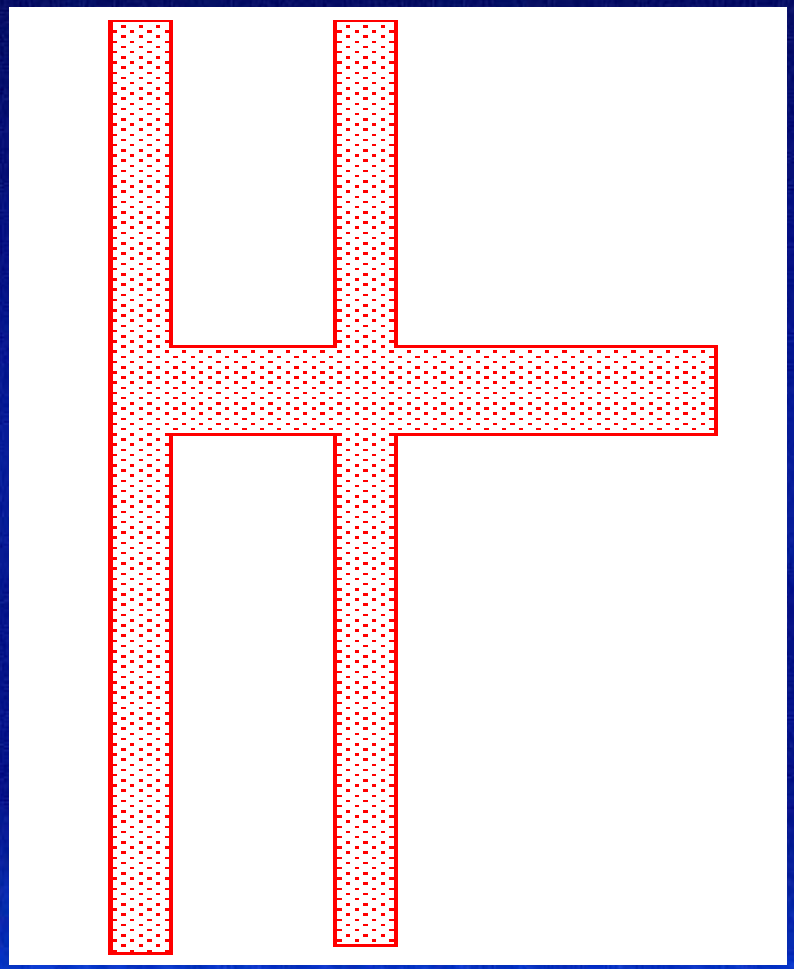
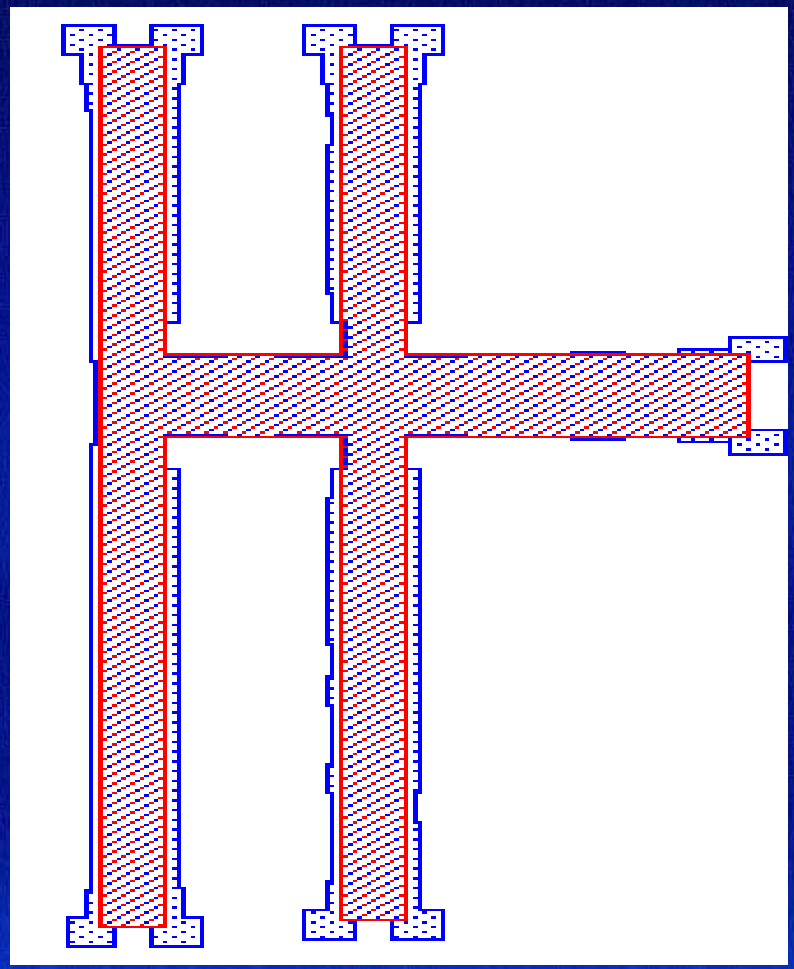
Growing Complexity

- **Process Complexity Factor:**
  - **Device count growing:**
    - **The billion + transistor trend and objective**
  - **Mask count growing:**
    - **increasing interconnect layers for RC performance**
    - **multiple device type**
  - **More complex OPC/correction on more layers**
- **Impact:**
  - **Data handling a growing problem:**
    - **Exponential data growths forecasted**
  - **Cost and TPT issues**

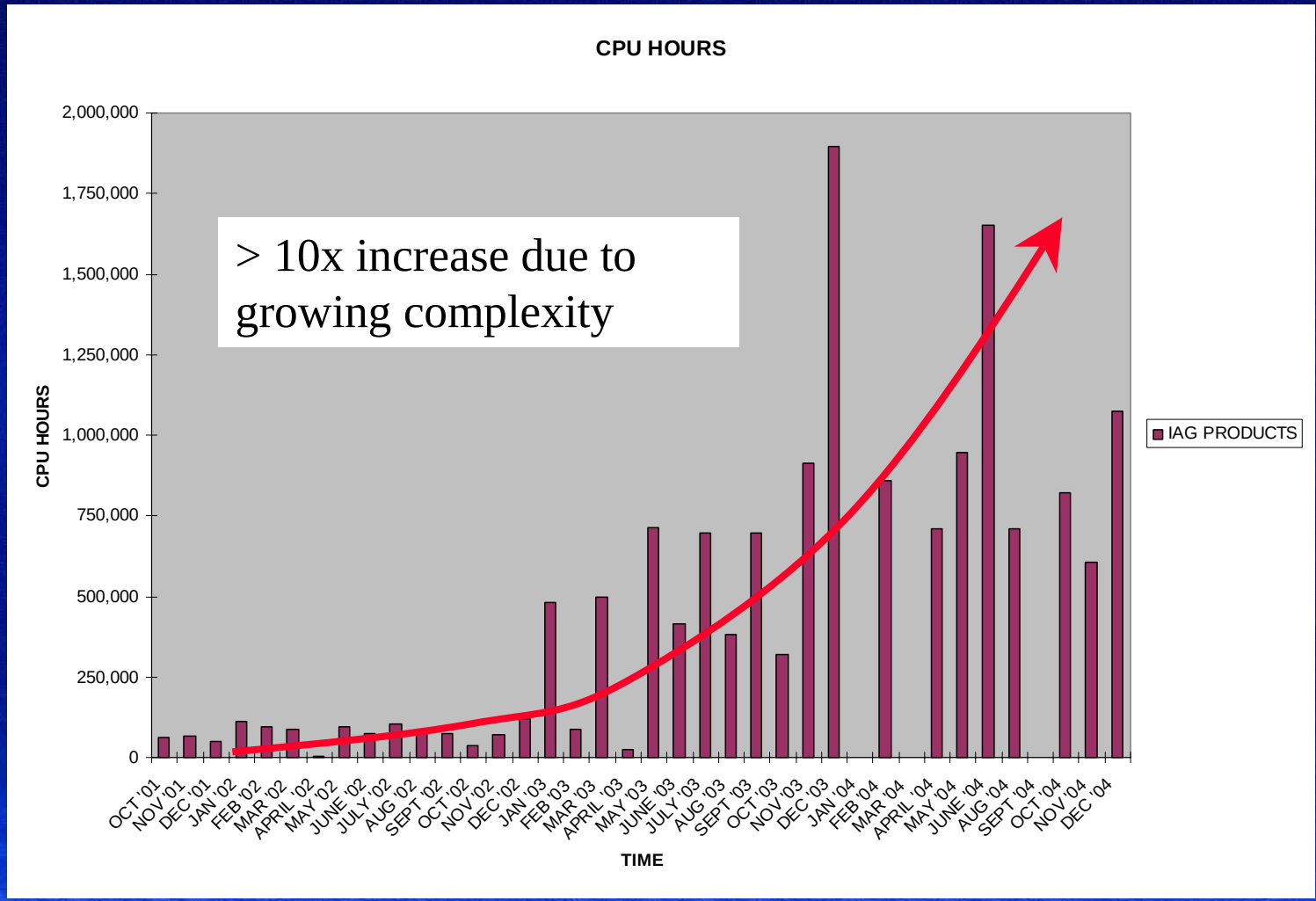
Data Complexity Increasing





6x increase in vertices

Trend In Total CPU Tapeout Hours



Strategies required to reduce impact of complexity

- Hierarchical, redundant database methods
- Simplified / improved design data structures
- Optimized correction, tapeout software
- Lower cost / scalable hardware solutions: e.g. clustered Linux IA

Conclusions

- **Transistor scaling alive and well: new Terahertz architecture**
  - Terahertz operation, Low power, Scalable beyond 65nm node
  - Key elements demonstrated
    - Depleted Substrate Transistor with raised source drain
    - High k gate, 15nm CMOS gate length

- Process and device control challenges threaten performance gains
  - Systematic WID variation growing in impact
  - Design and process solutions are possible and need to be pursued

- Data complexity and management challenge the billion transistor product
  - Layout, software and hardware solutions possible and required

- Overall, cost / benefit optimization will be required

Acknowledgements

- Keith Bowman
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